INTEGRATED CIRCUITS

DATA SHEET

74HC3G14; 74HCT3G14

Inverting Schmitt-triggers

Product specification

2002 Jul 23

Philips Semiconductors

PHILIPS

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Unlimited input rise and fall times
- Very small 8 pins package.

APPLICATIONS

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators
- Output capability: standard.

DESCRIPTION

The 74HC3G/HCT3G14 is a high-speed Si-gate CMOS device.

The 74HC3G/HCT3G14 provides three inverting buffers with Schmitt-trigger action. This device is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC3G14	HCT3G14	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 50 pF; V_{CC} = 4.5 V	16	21	ns
C_I	input capacitance		2	2	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	10	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total switching outputs;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For HC3G the condition is V_I = GND to V_{CC}.
   For HCT3G the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	**nY**
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3G14DP	–40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	H14
74HCT3G14DP	–40 to +125 °C	8	TSSOP-8	plastic	SOT505-2	T14

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input 1A
2	3Y	data output 3Y
3	2A	data input 2A
4	GND	ground (0 V)
5	2Y	data output 2Y
6	3A	data input 3A
7	1Y	data output 1Y
8	V_{CC}	supply voltage

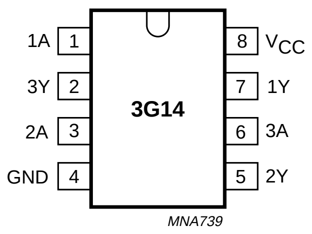


Fig.1 Pin configuration.

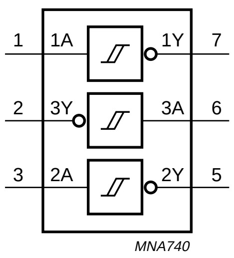


Fig.2 Logic symbol.

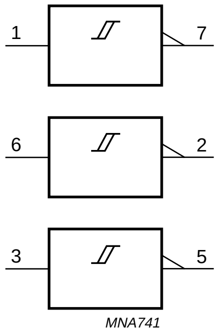


Fig.3 IEC logic symbol.

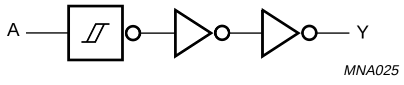


Fig.4 Logic diagram (one driver).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC3G14			74HCT3G14			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V; note 1	–	25	mA
I_{CC}	V_{CC} or GND current	note 1	–	50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

DC CHARACTERISTICS

Type 74HC3G14

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	6.0	5.9	6.0	–	5.9	–	5.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	4.5	4.18	4.32	–	4.13	–	3.7	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -5.2$ mA	6.0	5.68	5.81	–	5.63	–	5.2	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	2.0	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	6.0	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	4.5	–	0.15	0.26	–	0.33	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 5.2$ mA	6.0	–	0.16	0.26	–	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	6.0	–	–	1.0	–	10	–	20	μA

Type 74HCT3G14

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	4.5	4.18	4.32	–	4.13	–	3.7	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	4.5	–	0.15	0.26	–	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	1.0	–	10	–	20	μA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} - 2.1$ V; $I_O = 0$	4.5 to 5.5	–	–	300	–	375	–	410	μA

TRANSFER CHARACTERISTICS

Type 74HC3G14

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{T+}	positive going threshold voltage	see Figs. 5 and 6	2.0	1.0	1.18	1.5	1.0	1.5	1.0	1.5	V
			4.5	2.3	2.6	3.15	2.3	3.15	2.3	3.15	V
			6.0	3.0	3.46	4.2	3.0	4.2	3.0	4.2	V
V_{T-}	negative going threshold voltage	see Figs. 5 and 6	2.0	0.3	0.6	0.9	0.3	0.9	0.3	0.9	V
			4.5	1.13	1.47	2.0	1.13	2.0	1.13	2.0	V
			6.0	1.5	2.06	2.6	1.5	2.6	1.5	2.6	V
V_H	hysteresis voltage ($V_{T+} - V_{T-}$)	see Figs. 5 and 6	2.0	0.3	0.6	1.0	0.3	1.0	0.3	1.0	V
			4.5	0.6	1.13	1.4	0.6	1.4	0.6	1.4	V
			6.0	0.8	1.40	1.7	0.8	1.7	0.8	1.7	V

Type 74HCT3G14

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{T+}	positive going threshold voltage	see Figs. 5 and 6	4.5	1.2	1.58	1.9	1.2	1.9	1.2	1.9	V
			5.5	1.4	1.78	2.1	1.4	2.1	1.4	2.1	V
V_{T-}	negative going threshold voltage	see Figs. 5 and 6	4.5	0.5	0.87	1.2	0.5	1.2	0.5	1.2	V
			5.5	0.6	1.11	1.4	0.6	1.4	0.6	1.4	V
V_H	hysteresis voltage ($V_{T+} - V_{T-}$)	see Figs. 5 and 6	4.5	0.4	0.71	–	0.4	–	0.4	–	V
			5.5	0.4	0.67	–	0.4	–	0.4	–	V

TRANSFER CHARACTERISTIC WAVEFORMS

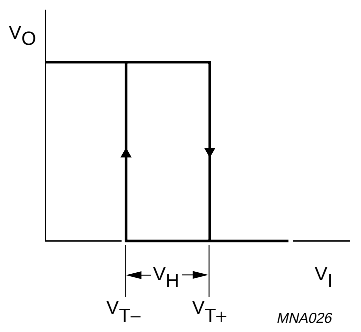
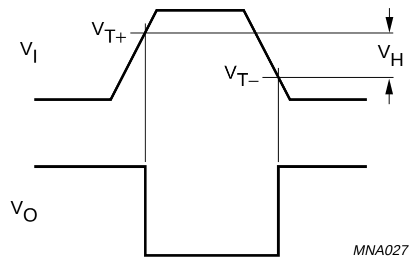
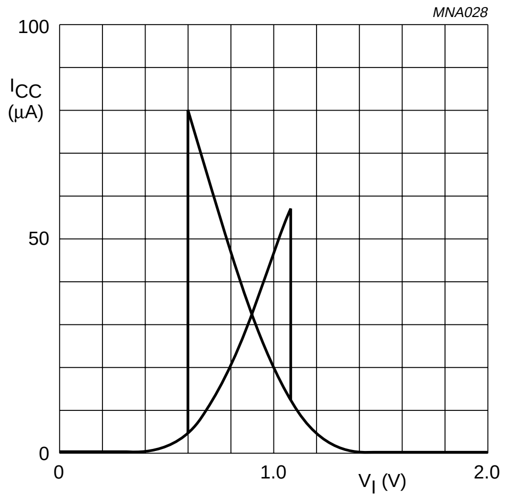


Fig.5 Transfer characteristic.



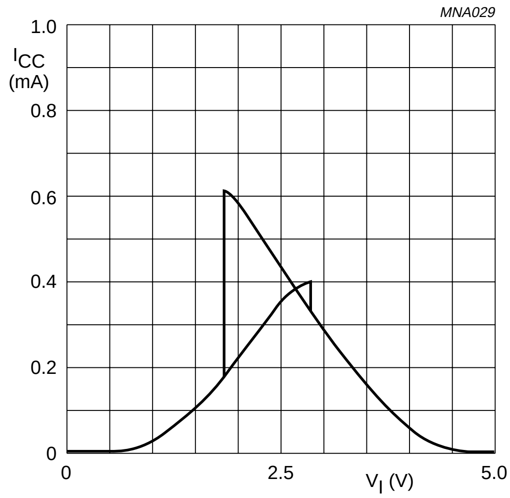
V_{T+} and V_{T-} are between limits of 20% and 70%.

Fig.6 The definitions of V_{T+}, V_{T-} and V_H



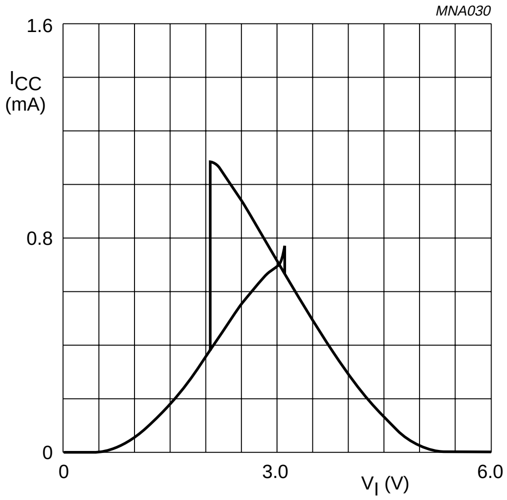
V_{CC} = 2.0 V.

Fig.7 Typical HC3G transfer characteristics.



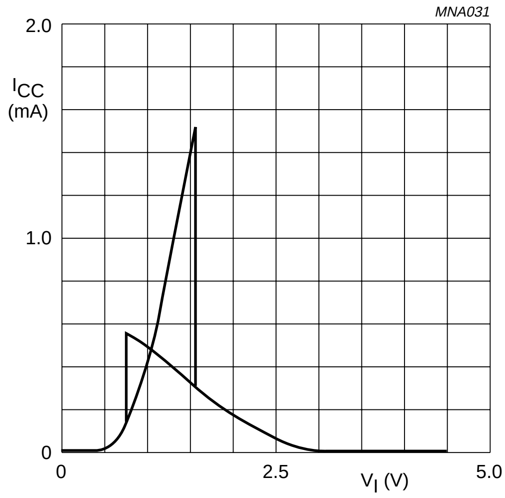
V_{CC} = 4.5 V.

Fig.8 Typical HC3G transfer characteristics.



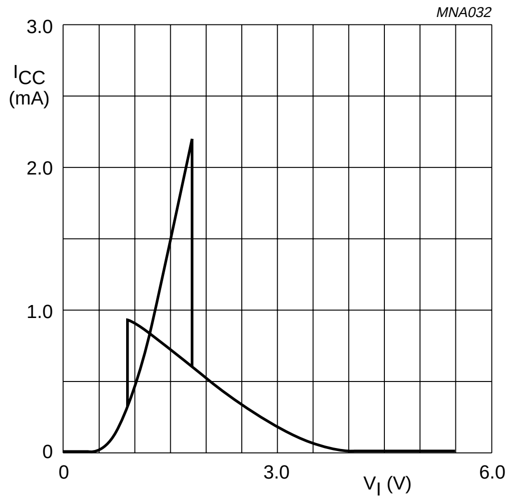
V_{CC} = 6.0 V.

Fig.9 Typical HC3G transfer characteristics.



V_{CC} = 4.5 V.

Fig.10 Typical HCT3G transfer characteristics.



V_{CC} = 5.5 V.

Fig.11 Typical HCT3G transfer characteristics;

AC CHARACTERISTICS

Type 74HC3G14

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

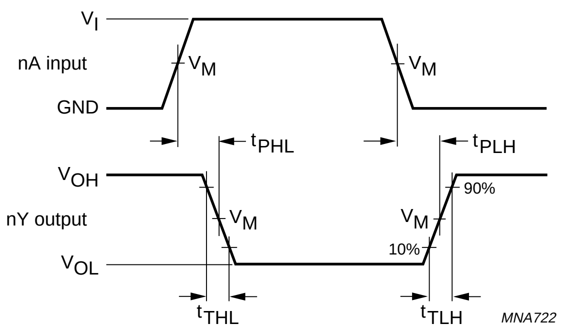
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 12 and 13	2.0	–	53	125	–	155	–	190	ns
			4.5	–	16	25	–	31	–	38	ns
			6.0	–	13	21	–	26	–	32	ns
t_{THL}/t_{TLH}	output transition time	see Figs 12 and 13	2.0	–	20	75	–	95	–	110	ns
			4.5	–	7	15	–	19	–	22	ns
			6.0	–	5	13	–	16	–	19	ns

Type 74HCT3G14

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

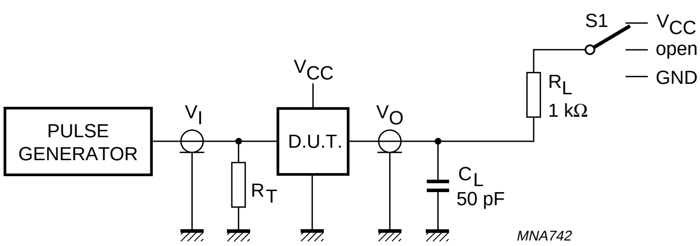
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 12 and 13	4.5	–	21	32	–	40	–	48	ns
t_{THL}/t_{TLH}	output transition time	see Figs 12 and 13	4.5	–	6	15	–	19	–	22	ns

AC WAVEFORMS



For HC3G: V_M = 50%; V_I = GND to V_{CC}.
For HCT3G: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.12 The input (nA) to output (nY) propagation delays and output transition times.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
C_L = load capacitance including jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.13 Load circuitry for switching times.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$

Where:

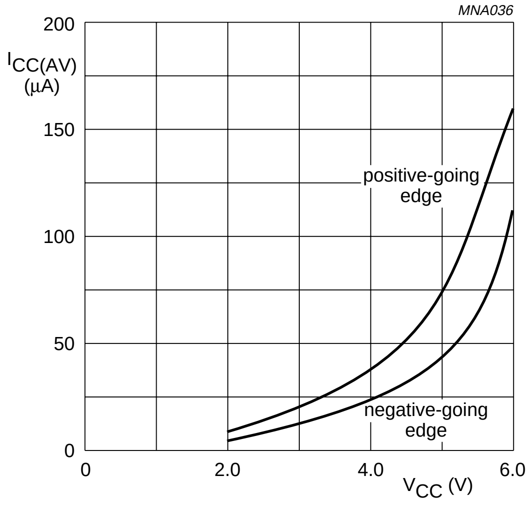
- P_{ad} = additional power dissipation (µW)
- f_i = input frequency (MHz)
- t_r = input rise time between 10% and 90% (ns);
- t_f = input fall time between 90% and 10% (ns);
- $I_{CC(AV)}$ = average additional supply current (µA).

Average I_{CCa} differs with positive or negative input transitions, as shown in Fig.14 and Fig.15.

HC3G14/HCT3G14 used in relaxation oscillator circuit, see Fig.16.

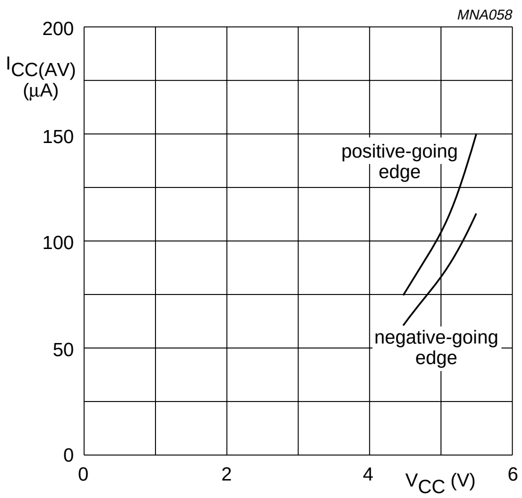
Remark to the application information

1. All values given are typical unless otherwise specified.



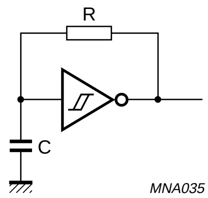
Linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.

Fig.14 Average I_{CC} for HC Schmitt-trigger devices.



Linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.

Fig.15 Average I_{CC} for HCT Schmitt-trigger devices.



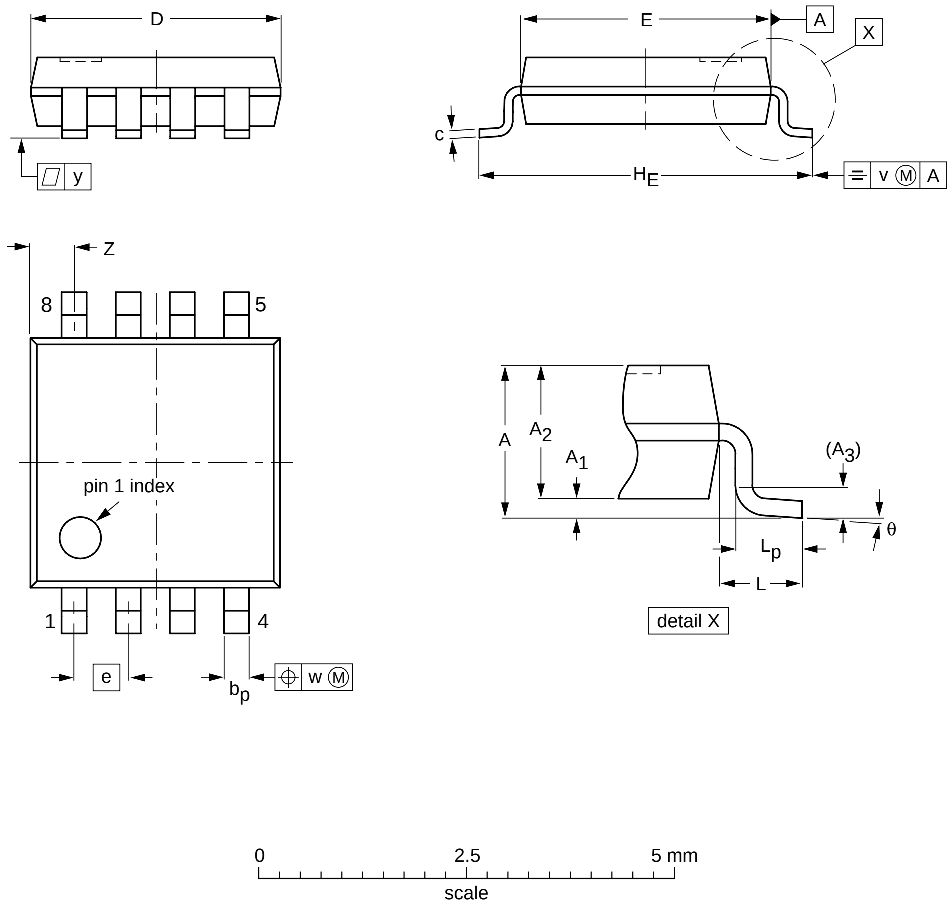
For HC3G: $f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$

For HCT3G: $f = \frac{1}{T} \approx \frac{1}{0.67 \times RC}$

Fig.16 Relaxation oscillator using the HC3G/HCT3G14.

PACKAGE OUTLINE

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

© Koninklijke Philips Electronics N.V. 2002 SCA74

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands 613508/01/pp20 Date of release: 2002 Jul 23 Document order number: 9397 750 09981

Let's make things better.

Philips Semiconductors

PHILIPS